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RN-6203

B. E. II (Sem. III) (Electrical) Examination

May / June – 2010

Electronics-I

Time : Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 3) (Electrical)**

Name of the Subject :

☛ **Electronics-1**

☛ Subject Code No. : **6 2 0 3** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Assume suitable data wherever necessary.
(4) Figures to the right indicate full marks.
(5) Use scientific calculator casio FX-82, 83, 100 or equivalent of any other comapny.

SECTION - I

1 (a) Answer the following in brief : **10**

(i) What is meant by the term "Barrier potential" ? What are its values for Si and Ge diodes ?

(ii) Does temperature affect breakdown voltage of diode ? Explain it.

(iii) Define and explain the significance of Ripple and form factors in relation with the rectifying circuits.

(iv) Define and explain the signficaince of common emitter amplification factor Bdc

(v) Why is CE configuration preferred over the other configuration ?

(b) Answer the following : **10**

(i) For the circit of **Fig. 1**, find $V_o(t)$ if $V_i(t)$ is

(a) Square wave with $\pm 10V$ amplitude

(b) Sine wave with 1V peak. Assume Ideal diode

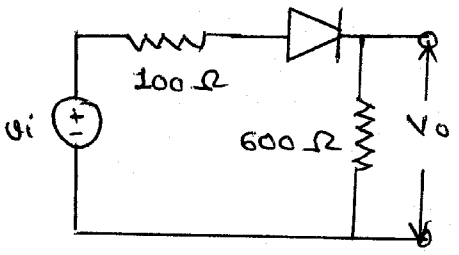


Fig. 1

(ii) State the regions of operation of transistor and explain the biasing condtion for the three regions.

2 (a) Draw the circuit diagram and explain the operation of a full wave rectifier and state its advantages and disadvantages **8**

(b) For the transistor shown in **Fig. 2**, β = 100, I_{CO} = 20 nA. Find the transistor currents and state in which region it is operating. Assume that it is a silicon transistor. **7**

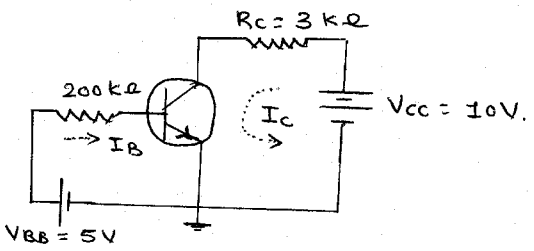


Fig. 2

OR

2 (a) Explain the function of emitter bypass capacitor. Draw AC and DC load lines for CE amplifier with bypass capacitors. **8**

(b) In a centre tapped full wave rectifier the rms half secondary voltage is 9V. Assuming ideal diodes and load resistance $R_L = 1k\Omega$ find : **7**

(i) Peak current

(ii) DC load voltage

(iii) RMS current

(iv) Ripple factor

(v) Effciency.

3 Write short notes on : (any **three**) **15**

(i) Potential Divider Bias

(ii) Schottcky diode

(iii) LC and PIE filters

(iv) Diode capacitance

(v) Input and output characteristic of NPN Transistor.

SECTION - II

4 (a) Answer the following : **10**

(i) Full form of BJT is _____.

(ii) True/False : BJT is current controlled device.

(iii) The reverse saturation current ICBO approximately doubles for every _____.

(iv) The saturation drain current IO in an FET is _____.

(v) True/False : Input impedance of JFET is greater than BJT but less than MOSFET.

(vi) The point of intersection of AC and DC load line is the _____.

(vii) Define amplification.

(viii) True/False : The maximum efficiency of class A power amplifier is 25%.

(ix) In class C amplifier Q point is well beyond the cut-off region. True/False.

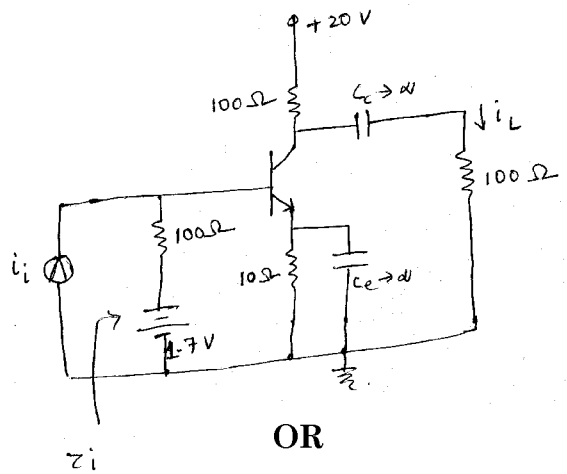
(x) What is the main application of CC configuration of transistor?

(b) (i) Explain working of class B push-pull power amplifier. Draw AC and DC load lines. **8**

(ii) Explain by graphical method how h_{oe} and h_{fe} parameters are obtained. **2**

5 (a) Explain the effect of temperature on Q-point. **8**

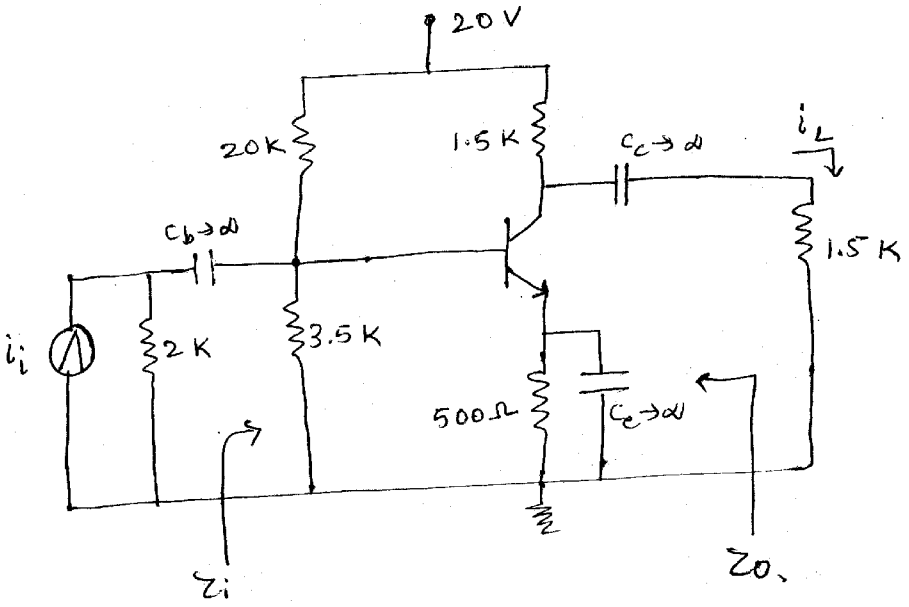
(b) For the given ckt $h_{re} = h_{oe} = 0$, $50 < h_{fe} < 150$, calculate the range of A_i and Z_i to be expected. **8**



OR

5 (a) Explain n-channel FET and its characterisation. 8

(b) For the Si transistor in figure h_{fe} = 100, $h_{re}=h_{oe}=0$. Find h_{ie}, A_i, Z_i, Z_o. 8



6 Attempt any **two** : 14

(i) Phase splitting ckt.

(ii) Compare BJT and FET. Classify FET devices.

(iii) Discuss the effect on Q-point due to variation in β.